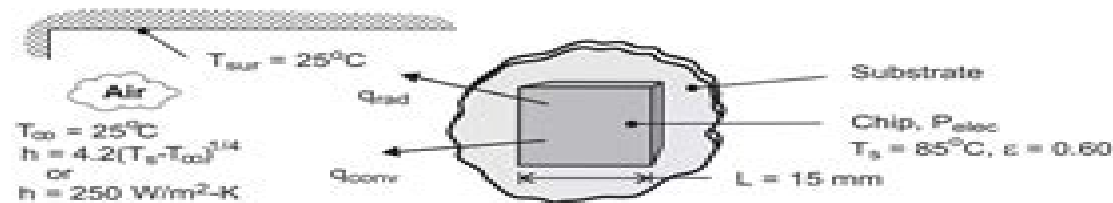


PROBLEM 1.31

KNOWN: Width, surface emissivity and maximum allowable temperature of an electronic chip. Temperature of air and surroundings. Convection coefficient.

FIND: (a) Maximum power dissipation for free convection with $h(\text{W/m}^2\cdot\text{K}) = 4.2(T - T_\infty)^{1/4}$, (b) Maximum power dissipation for forced convection with $h = 250 \text{ W/m}^2\cdot\text{K}$.

SCHEMATIC:



ASSUMPTIONS: (1) Steady-state conditions, (2) Radiation exchange between a small surface and a large enclosure, (3) Negligible heat transfer from sides of chip or from back of chip by conduction through the substrate.

ANALYSIS: Subject to the foregoing assumptions, electric power dissipation by the chip must be balanced by convection and radiation heat transfer from the chip. Hence, from Eq. (1.10),

$$P_{\text{elec}} = q_{\text{conv}} + q_{\text{rad}} = hA(T_s - T_\infty) + \epsilon A\sigma(T_s^4 - T_{\text{sur}}^4)$$

where $A = L^2 = (0.015\text{m})^2 = 2.25 \times 10^{-4} \text{ m}^2$.

(a) If heat transfer is by natural convection,

$$q_{\text{conv}} = C A (T_s - T_\infty)^{5/4} = 4.2 \text{ W/m}^2\cdot\text{K}^{5/4} \left(2.25 \times 10^{-4} \text{ m}^2 \right) (60\text{K})^{5/4} = 0.158 \text{ W}$$

$$q_{\text{rad}} = 0.60 \left(2.25 \times 10^{-4} \text{ m}^2 \right) 5.67 \times 10^{-8} \text{ W/m}^2\cdot\text{K}^4 \left(358^4 - 298^4 \right) \text{K}^4 = 0.065 \text{ W}$$

$$P_{\text{elec}} = 0.158 \text{ W} + 0.065 \text{ W} = 0.223 \text{ W}$$

<

(b) If heat transfer is by forced convection,

$$q_{\text{conv}} = hA(T_s - T_\infty) = 250 \text{ W/m}^2\cdot\text{K} \left(2.25 \times 10^{-4} \text{ m}^2 \right) (60\text{K}) = 3.375 \text{ W}$$

$$P_{\text{elec}} = 3.375 \text{ W} + 0.065 \text{ W} = 3.44 \text{ W}$$

<

COMMENTS: Clearly, radiation and natural convection are inefficient mechanisms for transferring heat from the chip. For $T_s = 85^\circ\text{C}$ and $T_\infty = 25^\circ\text{C}$, the natural convection coefficient is $11.7 \text{ W/m}^2\cdot\text{K}$. Even for forced convection with $h = 250 \text{ W/m}^2\cdot\text{K}$, the power dissipation is well below that associated with many of today's processors. To provide acceptable cooling, it is often necessary to attach the chip to a highly conducting substrate and to thereby provide an additional heat transfer mechanism due to conduction from the back surface.

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Table of Contents Solution Manual For Incropera

1. Understanding the eBook Solution Manual For Incropera
 - The Rise of Digital Reading Solution Manual For Incropera
 - Advantages of eBooks Over Traditional Books
2. Identifying Solution Manual For Incropera
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Solution Manual For Incropera
 - User-Friendly Interface
4. Exploring eBook Recommendations from Solution Manual For Incropera
 - Personalized Recommendations
 - Solution Manual For Incropera User Reviews and Ratings
 - Solution Manual For Incropera and Bestseller Lists
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 - Solution Manual For Incropera Enhanced eBook Features
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 - Highlighting and Note-Taking Solution Manual For Incropera
 - Interactive Elements Solution Manual For Incropera
- 8. Staying Engaged with Solution Manual For Incropera
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Solution Manual For Incropera
- 9. Balancing eBooks and Physical Books Solution Manual For Incropera
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Solution Manual For Incropera
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Solution Manual For Incropera
 - Setting Reading Goals Solution Manual For Incropera
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Solution Manual For Incropera
 - Fact-Checking eBook Content of Solution Manual For Incropera
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development

- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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