

```
1 .....
2 -- HEIG-VD, institute REDS, 1400 Yverdon-les-Bains
3 -- Project :
4 -- File   :
5 -- Autor  :
6 -- Date   :
7 --
8 .....
9 -- Description :
10 --
11 .....
12
13 library ieee;
14     use ieee.std_logic_1164.all;
15     --use ieee.numeric_std.all;
16
17 entity VHDL_Component is
18     port(
19         .....
20         --Insert input ports below
21         horloge_i  : in  std_logic;           -- input bit example
22         val_i       : in  std_logic_vector(3 downto 0); -- input vector example
23         .....
24         --Insert output ports below
25         max_o       : out std_logic;           -- output bit example
26         cot_o       : out std_logic_vector(3 downto 0) -- output vector example
```

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Sabine Zange

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