10EC021

M. Tech. Degree Examination, January 2011 **CMOS VLSI Design**

Time: 3 hrs.	
	Note: Answer any FIVE full questions.

Max. Marks:100

- a. Describe the construction, working and characteristics of enhancement mode MOSFET, with the relevant figure. Compare the characteristics of this MOSFET with depletion mode (10 Niarks) MOSFET.
 - b. Define the body effect in MOSSEFT. Derive the MOSFET current equation, in different (10 Marks) regions of operation.
- Explain the working of BICMOS inverter. State how the stored charges in the base are eliminated. Write the circuit diagram of BICMOS NAND gate. (DO Minirkes)
 - Describe the term tunneling and punch through in MOSFET. (04 Marks)
 - Briefly explain the pseudo nMOS inverter and the saturated load inverter, with their output (06 Marks) characteristics.
- What is meant by lamda based design rules? List the lamda based design rules for metal (03 Marks) layer, polysillicon layer and transistor. (08 Marks)
 - b. Describe with a neat sketch, pwell process for CMOS fabrication.
 - e. Derive the scaling factors for the following CMOS parameters : (04 Marks) ii) Gate delay Ta i) Gate capacitance C_e
- Explain the sheet resistance and standard unit capacitance. What is the effect of fluse parameter in delay unit 7?
 - b. Bring out the difference stick diagram and layout. Draw the schematic and layout diagram for the following functions.
 - ii) Y = AB + A B. i) Y = A + BC

(10 Marks)

- Explain the effect of parasitic capacitance in CMOS 2 input NOR gate. 694 Marks)
 - Prove that the switching threshold of NOR2 is VDD/2, when Ute = |Ute | and ke = UKe. cos Marko)
 - c. By constructing Euler graph, for the pull up and pull down device, draw the stick diagram for following logic function.
 - Z = A(D + E) + BC.

Also draw the optimized stick diagram for the same.

(10 Marks)

- Describe the behavior of bistable element. Derive the expression for the output voltage. (08 Marks)
 - What is clocked latch? Write and explain AOI based implementation of the clocked NOR post Minerkov). bussed SR lately.
 - Draw the dynamic CMOS logic and explain the pre-charge and evaluation mode. (84 Marks)
- What is pass transistor? Describe how does logic '0' transfer and logic '1' transfer takes (10 Marks) place in pass transistor.
 - Explain the different types of current mirror circuits. How can these be used in the design of (10 Marks) a differential amplifier?
- Write short notes on:
 - a. Differential inverter
 - Complementary pass logic
 - c. Domino logic

the Emplorate Note : 1. On completing your answers, computes ny taon ungaminates some seem 2. Any revealing of Mentification, appeal to evidence and for equations written in

Inpact ionization in MOS transistors.

(20 Mariko)

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