	MODEL NUMBER	V80-700	V80-1000	V80-1500	V80-2000
CAPACITY	Power rating	700VA (420W)	1000VA (600W)	1500VA (900W)	2000VA (1200W)
INPUT	Voltage nominal	120VAC			
	Voltage range	82-148VAC			
	Frequency	50/60Hz auto sensing			
OUTPUT	Voltage	120VAC			
	Waveform	Pure sine wave			
	Transfer time (typical)	2-6ms			
	Efficiency	Up to 96% ECO mode, 93% buck and boost mode			
	Harmonic distortion	2% @ 100% linear load; 5% @ 100% non-linear load			
BATTERY	Battery type	Sealed, maintenance-free lead acid			
	Battery quantity & size	(1) 12V 9AH	(2) 12V 7AH	(2) 12V 9AH	(2) 12V 9AH
	Charging current	1A max			
	Typical recharge	4 hours to 90%			
PHYSICAL	Dimensions (W x D x H)	17.2" x 16.1" x 3.5"			
	Weight	24 lbs	27.3 lbs	36.5 lbs	36.5 lbs
	Line cord (removable)	6ft, 5-15P to C13 6ft, 5-20P to C1			
	Receptacles	(8) NEMA 5-15R			
ENVIRONMENT	Operating temperature	32-104°F (0-40°C)			
	Audible noise	< 40d8A		< 45dBA	
	Altitude	11,500 ft above sea level			
APPROVALS		cTUVus, RoHs			
WARRANTY		3 years electronics, 3 years battery warranty (USA and Canada)			
COMMUNICATIONS INTERFACE		USB			
INCLUDED IN BOX		Line cord, tower pedestals, user manual, USB cable			
AVAILABLE OPTIONS		5 year extended warranty, bypass distribution (XBDM), power distribution (XPDU), 4-post rai kit, 2-post shelf kit, wall mount bracket			

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CL Gary

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book constitutes the refereed proceedings of the 10th International Conference on Algebraic Methodology and Software Technology AMAST 2004 held in Stirling Scotland UK in July 2004 The 35 revised full papers presented together with abstracts of 5 invited talks and an invited paper were carefully reviewed and selected from 63 submissions Among the topics covered are all current issues in formal methods related to algebraic approaches to software engineering including abstract data types process algebras algebraic specification model checking abstraction refinement model checking state machines rewriting Kleene algebra programming logic etc The Microarchitecture of Pipelined and Superscalar Computers Amos R. Omondi, 2013-03-09 This book is intended to serve as a textbook for a second course in the im plementation Le microarchitecture of computer architectures The subject matter covered is the collection of techniques that are used to achieve the highest performance in single processor machines these techniques center the exploitation of low level parallelism temporal and spatial in the processing of machine instructions. The target audience consists students in the final year of an undergraduate program or in the first year of a postgraduate program in computer science computer engineering or electrical engineering professional computer designers will also also find the book useful as an introduction to the topics covered Typically the author has used the material presented here as the basis of a full semester undergraduate course or a half semester post graduate course with the other half of the latter devoted to multiple processor machines The background assumed of the reader is a good first course in computer architecture and implementation to the level in say Computer Organization and Design by D Patterson and H Hennessy and familiarity with digital logic design The book consists of eight chapters The first chapter is an introduction to all of the main ideas that the following chapters cover in detail the topics covered are the main forms of pipelining used in high performance uniprocessors a taxonomy of the space of pipelined processors and performance issues It is also intended that this chapter should be readable as a brief stand alone survey

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