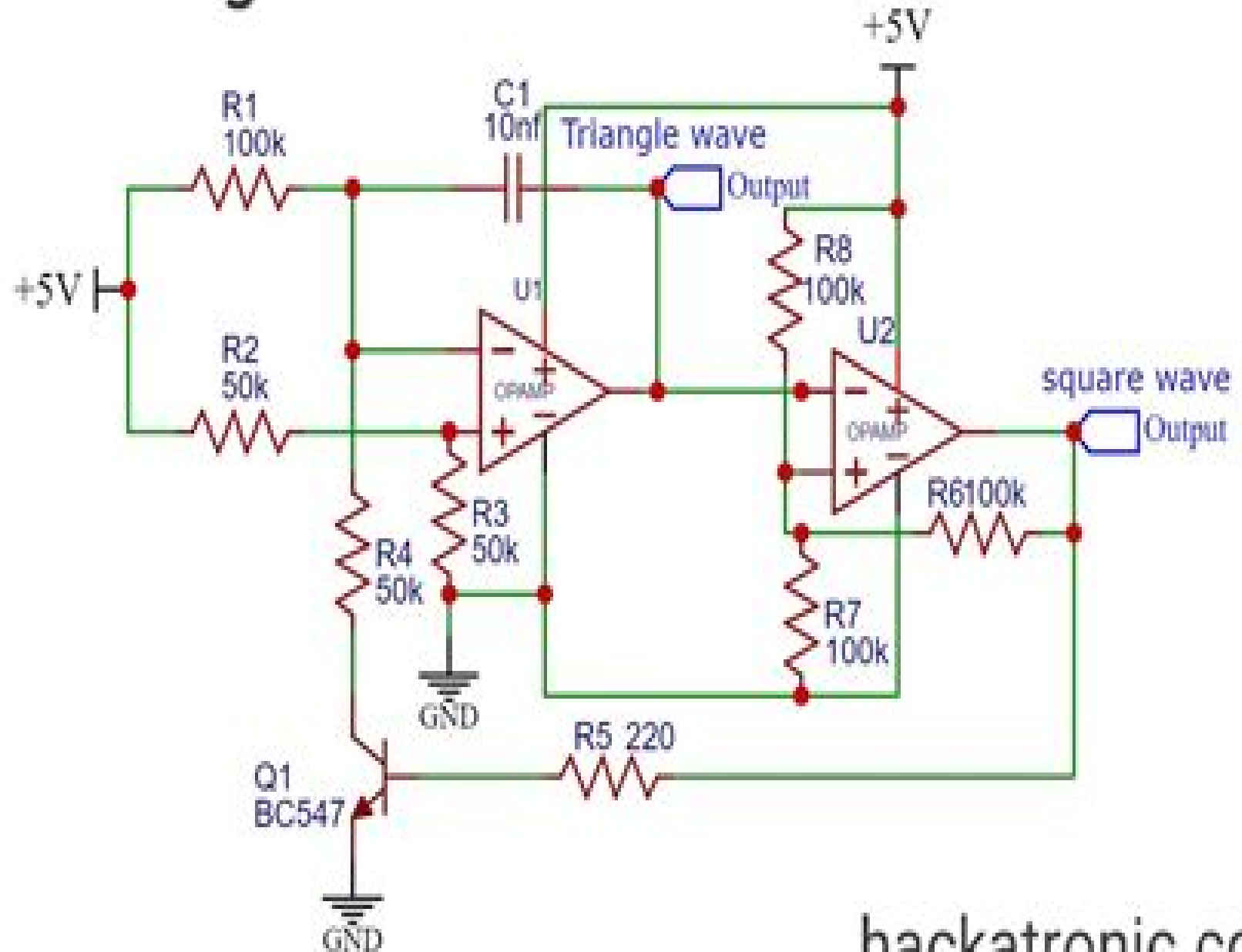


Voltage Controlled Oscillator Circuit



Voltage Controlled Oscillator

David Terrell



Voltage Controlled Oscillator:

Voltage Controlled Oscillator (VCO) Asim Mahmood Malik, 2000 **Voltage Controlled Oscillator (VCO) Technology**
Charles A. Bisseger, 1980 *Design of High-Performance CMOS Voltage-Controlled Oscillators* Liang Dai, Ramesh Harjani, 2012-12-06
Design of High Performance CMOS Voltage Controlled Oscillators presents a phase noise modeling framework for CMOS ring oscillators. The analysis considers both linear and nonlinear operation. It indicates that fast rail to rail switching has to be achieved to minimize phase noise. Additionally, in conventional design, the flicker noise in the bias circuit can potentially dominate the phase noise at low offset frequencies. Therefore, for narrow bandwidth PLLs, noise up conversion for the bias circuits should be minimized. We define the effective Q factor Q_{eff} for ring oscillators and predict its increase for CMOS processes with smaller feature sizes. Our phase noise analysis is validated via simulation and measurement results. The digital switching noise coupled through the power supply and substrate is usually the dominant source of clock jitter. Improving the supply and substrate noise immunity of a PLL is a challenging job in hostile environments such as a microprocessor chip where millions of digital gates are present. *A Digital Voltage-controlled Oscillator for Phase Lock Loops* Dominick E. Santarpia, 1968 *Design of High-Performance CMOS Voltage-Controlled Oscillators* Liang Dai, Ramesh Harjani, 2012-10-31
Design of High Performance CMOS Voltage Controlled Oscillators presents a phase noise modeling framework for CMOS ring oscillators. The analysis considers both linear and nonlinear operation. It indicates that fast rail to rail switching has to be achieved to minimize phase noise. Additionally, in conventional design, the flicker noise in the bias circuit can potentially dominate the phase noise at low offset frequencies. Therefore, for narrow bandwidth PLLs, noise up conversion for the bias circuits should be minimized. We define the effective Q factor Q_{eff} for ring oscillators and predict its increase for CMOS processes with smaller feature sizes. Our phase noise analysis is validated via simulation and measurement results. The digital switching noise coupled through the power supply and substrate is usually the dominant source of clock jitter. Improving the supply and substrate noise immunity of a PLL is a challenging job in hostile environments such as a microprocessor chip where millions of digital gates are present. **Voltage-controlled Oscillator (VCO) Design Used in Phase-locked Loops (PLLs) Based on CMOS Process** Chian Hin Teuu, 2003 **Distributed Voltage Controlled Oscillator** Sunil Modur Nagabhushana, 2001 *Design and Analysis 2.4 GHz Voltage-Controlled Oscillator (VCO) for Low-Phase Noise* Muhammad Fakhrulrazi Mohamad Fadzil, 2024
This project's scope is centred around the meticulous design and optimization of a Voltage Controlled Oscillator VCO with the specific target of achieving a stable oscillation frequency of 2.4 GHz. To realize this goal, the VCO will be meticulously crafted utilizing 0.35 μ m CMOS technology, which offers a robust foundation for integrated circuit design. A key emphasis of this design endeavor is the implementation of advanced filtering techniques to effectively eliminate extraneous noise sources, ultimately leading to improved phase noise performance. By harnessing the capabilities of CMOS technology and applying precise filtering strategies, this project seeks to

deliver a 2.4 GHz VCO that not only meets the frequency requirement but also excels in minimizing phase noise thereby enhancing its suitability for demanding wireless communication applications. The methodology employed in this study exclusively utilizes simulation techniques without involving any physical fabrication processes. Therefore, all results and findings herein are derived solely from computational simulations. It is essential to emphasize that no physical prototypes or fabricated components were utilized during this research. This research concentrates exclusively on design with simulation as the primary methodological approach. The scope of this study imposes constraints on physical fabrication processes. Consequently, the outcomes are derived solely from simulations conducted within the AWR Cadence software environment. While acknowledging the potential variance between simulated results and those obtained through physical implementation, it is worth noting that the simulations are expected to closely approximate the performance of the designed system under real-world conditions. However, it is imperative to recognize that the findings are contingent upon the virtual representation within the software.

thereby

Analog CMOS Voltage Controlled Oscillator (VCO) in Phase Locked Loop (PLL) Vern Shyn Khaw, 2005

A Voltage Controlled Oscillator/Mixer Marion C. Bartlett, Raymond C. Johnson, FLORIDA UNIV GAINESVILLE ENGINEERING AND INDUSTRIAL EXPERIMENT STATION., 1974

A new technique for product mixing of an input signal with a locally generated reference by using a voltage controlled oscillator VCO is described and verified both mathematically and experimentally. The technique consists of frequency modulating the oscillator with the signal voltage. It is shown that for low index frequency modulation by the signal, the sidebands of the oscillator produced by the signal are equivalent to those of a multiplicative mixer with a gain of approximately unity. The technique is particularly useful for synchronized IF correlator systems where a function generator can serve to generate the modulation waveform and act as a coherent detector.

simultaneously

Modified author abstract

RF and Microwave Transistor Oscillator Design Andrei Grebennikov, 2007-04-30

The increase of consumer electronics and communications applications using Radio Frequency (RF) and microwave circuits has implications for oscillator design. Applications working at higher frequencies and using novel technologies have led to a demand for more robust circuits with higher performance and functionality but decreased costs, size, and power consumption. As a result, there is also a need for more efficient oscillators. This book presents up-to-date information on all aspects of oscillator design, enabling a selection of the best oscillator topologies with optimized noise reduction and electrical performance. *RF and Microwave Transistor Oscillator Design* covers analyses of non-linear circuit design methods including spectral domain analysis, time domain analysis, and the quasilinear method; information on noise in oscillators; chapters on varactor and oscillator frequency tuning; CMOS voltage controlled oscillators and wideband voltage controlled oscillators; information on the stability of oscillations with discussions on the stability of multi-resonant circuits and the phase plane method; optimized design and circuit techniques beginning with the empirical and analytic design approaches; moving on to the high efficiency design technique; general operation and design principles of oscillators.

including a section on the historical aspects of oscillator configurations A valuable reference for practising RF and Microwave designers and engineers RF and Microwave Transistor Oscillator Design is also useful for lecturers advanced students and research and design R D personnel

The Voltage-controlled Oscillator Harizah Ismail,1994

Design of a Voltage Controlled Oscillator John Franklin Alexander,196?

Automatic Generation of an LC Voltage Controlled Oscillator Donghyeok Kil,2013 A Voltage Controlled Oscillator VCO is used to generate a signal with a frequency that is a function of an input voltage amplitude and is an integral part of circuits such as phase locked loops frequency synthesizers down conversion receivers and clock generators A typical design flow for a VCO involves architecture selection based on specification calculation of circuit parameters simulation and iterations of circuit parameters based on the simulation result In such a design flow changes in specification or process can lead to significant redesign This report focuses on a C based LC VCO generation software that seeks to automate the design process and that includes calculation of circuit parameters creation of Spectre netlist invocation of simulation automated checking of the result and a feedback mechanism to modify circuit parameters until the design can converge to the desired specification Object Oriented Programming principles such as inheritance polymorphism encapsulation class abstraction are exercised to maximize reusability and portability to other projects which may require different foundry device models and supply voltages

Voltage Controlled Oscillator Phase Noise Reduction Technique Céline E. M. Fletcher,2006

Low Phase Noise Voltage-controlled Oscillator Design Zhipeng Zhu,2005 Two kinds of voltage controlled oscillators VCO active inductor based VCO and LC cross coupled VCO are studied in this work Although the phase noise performance is not competitive the proposed active inductor based VCO provide an alternative method to VCO design with very small chip area and large tuning range The measurement shows a test oscillator based on active inductor topology successfully oscillates near 530MHz band The phase noise of the widely used LC cross coupled VCO is extensively investigated in this work Under the widely used power dissipation and chip area constraints a novel optimization procedure in LC oscillator design centered on a new inductance selection criterion is proposed This optimization procedure is based on a physical phase noise model From it several closed form expressions are derived to describe the phase noise generated in the LC oscillators which indicate that the phase noise is proportional to the L^2/gL^3 factor The minimum value of this factor for an area limited spiral inductor is proven to monotonically decrease with increasing inductance suggesting a larger inductance is helpful to reduce the phase noise in LC VCO design The validity of the optimization procedure is proven by simulations Two test chips are designed and measured

A Design and Analysis of High Performance Voltage Controlled Oscillators Bin Wan,2006

Op Amps: Design, Application, and Troubleshooting David Terrell,1996 Basic concepts of the integrated operational amplifier Amplifiers Voltage comparators Oscillators Active filters Power supply circuits Signal processing circuits Digital to analog and analog to digital conversion Arithmetic function circuits Nondideal op amp characteristics Specialized devices

Design of VCO-based ADCs Vishnu

Unnikrishnan, 2017-03-28 Today's complex electronic systems with billions of transistors on a single die are enabled by the aggressive scaling down of the device feature size at an exponential rate as predicted by the Moore's law. Digital circuits benefit from technology scaling to become faster, more energy efficient as well as more area efficient as the feature size is scaled down. Moreover, digital design also benefits from mature CAD tools that simplify the design and cross technology porting of complex systems leveraging on a cell based design methodology. On the other hand, the design of analog circuits is getting increasingly difficult as the feature size scales down into the deep nanometer regime due to a variety of reasons like shrinking voltage headroom, reducing intrinsic gain of the devices, increasing noise coupling between circuit nodes due to shorter distances etc. Furthermore, analog circuits are still largely designed with a full custom design flow that makes their design and porting tedious, slow and expensive. In this context, it is attractive to consider realizing analog mixed signal circuits using standard digital components. This leads to scaling friendly mixed signal blocks that can be designed and ported using the existing CAD framework available for digital design. The concept is already being applied to mixed signal components like frequency synthesizers where all digital architectures are synthesized using standard cells as basic components. This can be extended to other mixed signal blocks like digital to analog and analog to digital converters as well, where the latter is of particular interest in this thesis. A voltage controlled oscillator (VCO) based analog to digital converter (ADC) is an attractive architecture to achieve all digital analog to digital conversion due to favorable properties like shaping of the quantization error, inherent anti alias filtering etc. Here a VCO operates as a signal integrator as well as a quantizer. A converter employing a ring oscillator as the VCO lends itself to an all digital implementation. In this dissertation, we explore the design of VCO based ADCs synthesized using digital standard cells with the long term goal of achieving high performance data converters built from low accuracy switch components. In a first step, an ADC is designed using vendor supplied standard cells and fabricated in a 65 nm CMOS process. The converter delivers an 8 bit ENOB over a 25 MHz bandwidth while consuming 3.3 mW of power, resulting in an energy efficiency of 235 fJ/step/Walden FoM. Then we utilize standard digital CAD tools to synthesize converter designs that are fully described using a hardware description language. A polynomial based digital post processing scheme is proposed to correct for the VCO nonlinearity. In addition, pulse modulation schemes like delta modulation and asynchronous sigma delta modulation are used as a signal pre coding scheme in an attempt to reduce the impact of VCO nonlinearity on converter performance. In order to investigate the scaling benefits of all digital data conversion, a VCO based converter is designed in a 28 nm CMOS process. The design delivers a 13.4 bit ENOB over a 5 MHz bandwidth, achieving an energy efficiency of 4.3 fJ/step according to post synthesis schematic simulation, indicating that such converters have the potential of achieving good performance in deeply scaled processes by exploiting scaling benefits. Furthermore, large conversion errors caused by non ideal sampling of the oscillator phase are studied. An encoding scheme employing one's counters is proposed to code the sampled ring oscillator output into a number which is resilient to a class of

sampling induced errors modeled by temporal reordering of the transitions in the ring The proposed encoding reduces the largest error caused by random reordering of up to six subsequent bits in the sampled signal from 31 to 2 LSBs Finally the impact of process voltage and temperature PVT variations on the performance while operating the converter from a subthreshold supply is investigated PVT adaptive solutions are suggested as a means to achieve energy efficient operation over a wide range of PVT conditions

A Low Power Low Phase Noise Voltage Controlled Oscillator Kriyang Shah, 2009 The explosive growth in wireless communication has driven research into low cost low power and miniaturised wireless receivers A low power and low phase noise voltage controlled oscillator VCO is one of the key components of transceiver systems Close in phase noise responsible for jitter in time domain is the most important parameter of a VCO as it results in inter symbol interferences in high speed analogue to digital converters ADCs VCO phase noise also degrades system sensitivity and selectivity of wireless receivers To improve battery life VCO designs for wireless receivers must consume the least possible power Hence the primary aims of this research are to achieve a VCO with very low close in phase noise and with low power consumption Substantial research into VCO topologies and the design of on chip passive elements has made on chip complementary metal oxide semiconductor CMOS implementation of LC tank VCO possible However the principle issues with CMOS LC VCOs have been the unavailability of a high quality factor Q on chip inductor and high flicker noise of active devices

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Voltage Controlled Oscillator Introduction

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