

First Semester M.Tech. Degree Examination, June/July 2015
Digital VLSI Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions.

1.
 - a. Discuss gradual channel approximation concept in MOSFET and derive the current expression for MOSFET operating in saturation region. (10 Marks)
 - b. Discuss the second order effects of MOSFET and arrive at current expression for MOSFET in saturation region considering channel length modulation. (06 Marks)
 - c. Discuss how constant voltage scaling affects the current and power characteristics of MOSFET. (04 Marks)
2.
 - a. Discuss the voltage transfer characteristics of CMOS inverter mentioning the regions of operation and input and output voltages. (06 Marks)
 - b. Calculate V_{TH} for a CMOS inverter when $k_n = k_p$, $k_n = 2 k_p$ and $k_n = k_p/2$ with $V_{T_{on}} = 0.6 V$, $V_{T_{op}} = -0.7 V$ and $V_{DD} = 3.3 V$. From the calculations, discuss how variations in k_n and k_p affects V_{TH} ? (08 Marks)
 - c. With the neat schematic, mention the parasitic capacitances in the CMOS inverter? (06 Marks)
3.
 - a. Explain the concept of voltage bootstrapping. (05 Marks)
 - b. Discuss the charge sharing problem in CMOS circuits. Explain the various techniques used in domino CMOS logic for solving charge sharing problem. (10 Marks)
 - c. Design negative edge triggered D – Flipflop using true single phase clock (TSPC) dynamic CMOS logic. (05 Marks)
4.
 - a. Design 4×8 NOR based ROM array that can store the following data given in table 4(a).
 Note : $R_1, R_2, R_3, R_4 \rightarrow$ Address and $C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8 \rightarrow$ Memory Locations. (06 Marks)

R_1	R_2	R_3	R_4	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
1	0	0	0	0	1	0	1	0	1	0	0
0	1	0	0	1	1	1	0	0	1	0	0
0	0	1	0	1	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	0	1	1	1
- b. Draw a neat schematic of 6 T SRAM cell and discuss write '0' and read '0' operation? (10 Marks)
 - c. Explain the working principle of 3T DRAM cell. (04 Marks)
5.
 - a. Discuss CMOS switching power dissipation and derive the expression for average switching power dissipation. (06 Marks)
 - b. CMOS circuit consisting of 20 nodes with power consuming voltage transition (α_T) per clock cycle consumes a power of $10 \mu W$ for a give $C_{load} = 0.1 pF$ and $V_{DD} = 1.8 V$. Find the maximum operating frequency of the CMOS circuit if the node transitions is increased from 20 to 30. What is the change in switching power dissipation? (08 Marks)
 - c. Discuss briefly variable threshold CMOS and multi threshold CMOS circuits. (06 Marks)

Vlsi Design Question Papers

**Rakesh Kumar Garg,Ashish
Dixit,Pavan Yadav**



Vlsi Design Question Papers:

VLSI Design K. Lal Kishore, V. S. V. Prabhakar, 2013-12-30 Aimed primarily for undergraduate students pursuing courses in VLSI design the book emphasizes the physical understanding of underlying principles of the subject It not only focuses on circuit design process obeying VLSI rules but also on technological aspects of Fabrication VHDL modeling is discussed as the design engineer is expected to have good knowledge of it Various Modeling issues of VLSI devices are focused which includes necessary device physics to the required level With such an in depth coverage and practical approach practising engineers can also use this as ready reference Key features Numerous practical examples Questions with solutions that reflect the common doubts a beginner encounters Device Fabrication Technology Testing of CMOS device BiCMOS Technological issues Industry trends Emphasis on VHDL

Basic Electronics Rakesh Kumar Garg, Ashish Dixit, Pavan Yadav, 2008 **Principles of VLSI and CMOS Integrated Circuits** Jain Richa & Rai Amrita, 2016 For B E B Tech students of all Technical Universities Microelectronics VLSI Design is an emerging subject in the field of electronics in recent years It is an introductory source to internal parts of electronics at minute level This book is covering CMOS Design from a digital system level to circuit level and providing a background in CMOS Processing Technology The book includes basic theoretical knowledge as well as good engineering practice This book is recommended for B Tech M Tech and diploma students of all Indian Universities and also useful for competitive examinations

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System on Chip (SOC) Architecture Veena S. Chakravarthi,Shivananda R. Koteswarar,2023-08-14 This book deals with a practical approach to defining a system on a chip SoC architecture It is written by practicing industry experts with cumulative five decades of hands on experience The book discusses how the system level design challenges are addressed at the architecture stage and clearly defines different SoC subsystems and components The book explains the practical method of determining system subsystems in system architectures System on Chip SOC Architecture A Practical Approach provides readers with a complete understanding of methods for defining SoC architecture

Applications of Computational Intelligence Alvaro David Orjuela-Cañón,Juan Carlos Figueroa-García,Julián David Arias-Londoño,2018-12-13 This book constitutes the thoroughly refereed proceedings of the First IEEE Colombian

Conference ColCACI 2018 held in Medellin Colombia in May 2018 The 17 full papers presented were carefully reviewed and selected from 60 submissions The papers are organized in topical sections on artificial neural networks computational intelligence computer science

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VLSI-SoC: System-on-Chip in the Nanoscale Era - Design, Verification and Reliability Thomas Hollstein,Jaan Raik,Sergei Kostin,Anton Tšertov,Ian O'Connor,Ricardo Reis,2017-08-31 This book contains extended and revised versions of the best papers presented at the 24th IFIP WG 10 5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2016 held in Tallinn Estonia in September 2016 The 11 papers included in the book were carefully reviewed and selected from the 36 full papers presented at the conference The papers cover a wide range of topics in VLSI technology and advanced research They address the latest scientific and industrial results and developments as well as future trends in the field of System on Chip SoC Design

VLSI Design and Test Brajesh Kumar Kaushik,Sudeb Dasgupta,Virendra Singh,2017-12-21 This book constitutes the refereed proceedings of the 21st International Symposium on VLSI Design and Test VDAT 2017 held in Roorkee India in June July 2017 The 48 full papers presented together with 27 short papers were carefully reviewed and selected from 246 submissions The papers were organized in topical sections named digital design analog mixed signal VLSI testing devices and technology VLSI architectures emerging technologies and memory system design low power design and test RF circuits architecture and CAD and design verification

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