CHAPTER 1 INTRODUCTION

- 1.1 An ADD/SUBTRACT logic circuit is shown below. It performs the ADD operation for P = 0, and SUBTRACT for P = 1.
 - (a) Draw an equivalent CMOS logic diagram by noting that most CMOS gates, except for transmission gate and XOR, are inverting. For example, AND gate is implemented with NAND followed by an inverter.
 - (b) By using the gate array platform given on page 47, implement the CMOS circuit as compactly as possible with the aspect ratio, which is the ratio of vertical dimension to horizontal dimension, as close to 1 as possible.



Figure P14.1(a)

SOLUTION:

(b) The CMOS circuit implementation using the gate array platform:

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J Ma

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Solution Manual to Accompany CMOS Digital Integrated Circuits: Analysis and Design, Second Edition Sung-Mo Embedded SoPC Design with Nios II Processor and VHDL Examples Pong P. Chu, 2011-08-29 Kang, Yusuf Leblebici, 1999 The book is divided into four major parts Part I covers HDL constructs and synthesis of basic digital circuits Part II provides an overview of embedded software development with the emphasis on low level I O access and drivers Part III demonstrates the design and development of hardware and software for several complex I O peripherals including PS2 keyboard and mouse a graphic video controller an audio codec and an SD secure digital card Part IV provides three case studies of the integration of hardware accelerators including a custom GCD greatest common divisor circuit a Mandelbrot set fractal circuit and an audio synthesizer based on DDFS direct digital frequency synthesis methodology The book utilizes FPGA devices Nios II soft core processor and development platform from Altera Co which is one of the two main FPGA manufactures Altera has a generous university program that provides free software and discounted prototyping boards for educational institutions details at www altera com university The two main educational prototyping boards are known as DE1 99 and DE2 269 All experiments can be implemented and tested with these boards A board combined with this book becomes a turn key solution for the SoPC design experiments and projects Most HDL and C codes in the book are device independent and can be adapted by other prototyping boards as long as a board has similar I O configuration Embedded SoPC Design with Nios II Processor and Verilog Examples Pong P. Chu, 2012-05-14 Explores the unique hardware programmability of FPGA based embedded systems using a learn by doing approach to introduce the concepts and techniques for embedded SoPC design with Verilog An SoPC system on a programmable chip integrates a processor memory modules I O peripherals and custom hardware accelerators into a single FPGA field programmable gate array device In addition to the customized software customized hardware can be developed and incorporated into the embedded system as well allowing us to configure the soft core processor create tailored I O interfaces and develop specialized hardware accelerators for computation intensive tasks Utilizing an Altera FPGA prototyping board and its Nios II soft core processor Embedded SoPC Design with Nios II Processor and Verilog Examples takes a learn by doing approach to illustrate the hardware and software design and development process by including realistic projects that can be implemented and tested on the board Emphasizing hardware design and integration throughout the book is divided into four major parts Part I covers HDL and synthesis of custom hardware Part II introduces the Nios II processor and provides an overview of embedded software development Part III demonstrates the design and development of hardware and software of several complex I O peripherals including a PS2 keyboard and mouse a graphic video controller an audio codec and an SD secure digital card Part IV provides several case studies of the integration of hardware accelerators including a custom GCD greatest common divisor circuit a Mandelbrot set fractal circuit and an audio synthesizer based on DDFS direct digital frequency synthesis methodology While designing and developing an

embedded SoPC can be rewarding the learning can be a long and winding journey This book shows the trail ahead and guides readers through the initial steps to exploit the full potential of this emerging methodology FPGA Prototyping by VHDL Examples Pong P. Chu,2011-09-20 This book uses a learn by doing approach to introduce the concepts and techniques of VHDL and FPGA to designers through a series of hands on experiments FPGA Prototyping by VHDL Examples provides a collection of clear easy to follow templates for quick code development a large number of practical examples to illustrate and reinforce the concepts and design techniques realistic projects that can be implemented and tested on a Xilinx prototyping board and a thorough exploration of the Xilinx PicoBlaze soft core microcontroller Solutions Manual for Digital Integrated Circuits Ayers John E,2003-09 Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Vassilis Paliouras, Johan Vounckx, Diederik Verkest, 2005-08-25 Welcome to the proceedings of PATMOS 2005 the 15th in a series of international workshops

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Digital Integrated Circuits Jan M. Rabaey, Anantha P. Chandrakasan, Borivoje Nikolić, 2003 Intended for use in undergraduate senior level digital circuit design courses with advanced material sufficient for graduate level courses Progressive in content and form this text successfully bridges the gap between the circuit perspective and system perspective of digital integrated circuit design Beginning with solid discussions on the operation of electronic devices and in depth analysis of the nucleus of digital design the text maintains a consistent logical flow of subject matter throughout The revision addresses today s most significant and compelling industry topics including the impact of interconnect design for low power issues in timing and clocking design methodologies and the tremendous effect of design automation on the digital

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Table of Contents Solution Manual Digital Integrated Circuits Rabaey

- 1. Understanding the eBook Solution Manual Digital Integrated Circuits Rabaey
 - The Rise of Digital Reading Solution Manual Digital Integrated Circuits Rabaey
 - Advantages of eBooks Over Traditional Books
- 2. Identifying Solution Manual Digital Integrated Circuits Rabaey
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
- 3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Solution Manual Digital Integrated Circuits Rabaey
 - User-Friendly Interface
- 4. Exploring eBook Recommendations from Solution Manual Digital Integrated Circuits Rabaey
 - Personalized Recommendations
 - Solution Manual Digital Integrated Circuits Rabaey User Reviews and Ratings
 - Solution Manual Digital Integrated Circuits Rabaey and Bestseller Lists
- 5. Accessing Solution Manual Digital Integrated Circuits Rabaey Free and Paid eBooks
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- Solution Manual Digital Integrated Circuits Rabaey Budget-Friendly Options
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 - Solution Manual Digital Integrated Circuits Rabaey Enhanced eBook Features
- 7. Enhancing Your Reading Experience
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 - Highlighting and Note-Taking Solution Manual Digital Integrated Circuits Rabaey
 - Interactive Elements Solution Manual Digital Integrated Circuits Rabaey
- 8. Staying Engaged with Solution Manual Digital Integrated Circuits Rabaey
 - o Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Solution Manual Digital Integrated Circuits Rabaey
- 9. Balancing eBooks and Physical Books Solution Manual Digital Integrated Circuits Rabaey
 - Benefits of a Digital Library
 - o Creating a Diverse Reading Collection Solution Manual Digital Integrated Circuits Rabaey
- 10. Overcoming Reading Challenges
 - $\circ\,$ Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Solution Manual Digital Integrated Circuits Rabaey
 - Setting Reading Goals Solution Manual Digital Integrated Circuits Rabaey
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Solution Manual Digital Integrated Circuits Rabaey
 - Fact-Checking eBook Content of Solution Manual Digital Integrated Circuits Rabaey
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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