

CS-200: Verilog Coding Style Guide

Learning Goal: Verilog Style.

Requirements: Verible.

1 Introduction

This document will teach you some guidelines for a readable and well-constituted Verilog.

We will use [Verible](#) as the linting tool for the labs. The tool does not cover all of the rules in this document; however, it comes in handy in detecting many problems that might exist in your Verilog code. We will run Verible on each submission and will **deduct half of the lab grade** if the code does not pass the linting with zero errors. We provide a `flags.txt` file alongside this document that shall be used as a configuration input to the Verible linter. The content of the `flags.txt` file can be found below with the command needed to run the linter on a Verilog file.

```
-always-comb
+port-name-suffix
signal-name-style="style_regex:[a-z_0-9]+'"
-explicit-parameter-storage-type
+parameter-name-style="localparam_style:ALL_CAPS;parameter_style:ALL_CAPS"
```

```
verible-verilog-lint {file} --rules_config flags.txt
```

2 General Guidelines

- **always@ (*)** is used to describe a block with combinational logic. The `*` symbol is used in the sensitivity list to trigger the block whenever any of the inputs are changed; therefore, the outputs reflect the inputs change.
- **always@ (posedge clk)** is used to describe a block with sequential logic i.e., has flip-flops. The two keywords **posedge** and **negedge** determine whether the active clock edge of the flip-flops is the rising or the falling clock edge respectively.
- Use blocking (`=`) assignments in **combinational** always blocks.
- Use nonblocking (`<=`) assignments in **edge-sensitive sequential** always blocks. Blocking assignments (`=`) are not allowed.
- Avoid latches in your sequential designs and use only D flip-flops. Latches might sneak into your combinational blocks; to avoid this, it is a good practice to start your combinational always block

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Verilog Style Guide:

SystemVerilog For Design Stuart Sutherland, Simon Davidmann, Peter Flake, 2013-12-01 SystemVerilog is a rich set of extensions to the IEEE 1364 2001 Verilog Hardware Description Language Verilog HDL These extensions address two major aspects of HDL based design First modeling very large designs with concise accurate and intuitive code Second writing high level test programs to efficiently and effectively verify these large designs This book SystemVerilog for Design addresses the first aspect of the SystemVerilog extensions to Verilog Important modeling features are presented such as two state data types enumerated types user defined types structures unions and interfaces Emphasis is placed on the proper usage of these enhancements for simulation and synthesis A companion to this book SystemVerilog for Verification covers the second aspect of SystemVerilog

SystemVerilog for Verification Chris Spear, 2008-04-22 SystemVerilog for Verification Second Edition provides practical information for hardware and software engineers using the SystemVerilog language to verify electronic designs The author explains methodology concepts for constructing testbenches that are modular and reusable The book includes extensive coverage of the SystemVerilog 3.1a constructs such as classes program blocks randomization assertions and functional coverage It also reviews SystemVerilog 3.0 topics such as interfaces and data types This second edition contains a new chapter that covers programs and interfaces as well as chapters with updated information on directed testbench and OOP layered and random testbench for an ATM switch This edition also includes a new chapter that covers Interfacing to C and many new and improved examples and explanations For hardware engineers the book has several chapters with detailed explanations of Object Oriented Programming based on years of teaching OOP to hundreds of students For software engineers there is a wealth of information on testbenches multithreaded code and interfacing to hardware designs The reader only needs to know the Verilog 1995 standard The complete book that covers verification concepts and use of system verilog in Verification taking your from an easy start to advanced concepts with ease Paul D Franzon Alumni Distinguished Professor of ECE North Carolina State University

Digital System Design with SystemVerilog Mark Zwolinski, 2009-10-23 The Definitive Up to Date Guide to Digital Design with SystemVerilog Concepts Techniques and Code To design state of the art digital hardware engineers first specify functionality in a high level Hardware Description Language HDL and today s most powerful useful HDL is SystemVerilog now an IEEE standard Digital System Design with SystemVerilog is the first comprehensive introduction to both SystemVerilog and the contemporary digital hardware design techniques used with it Building on the proven approach of his bestselling Digital System Design with VHDL Mark Zwolinski covers everything engineers need to know to automate the entire design process with SystemVerilog from modeling through functional simulation synthesis timing simulation and verification Zwolinski teaches through about a hundred and fifty practical examples each with carefully detailed syntax and enough in depth information to enable rapid hardware design and verification All examples are available for download from the book s companion Web site zwolinski.org Coverage includes

Using electronic design automation tools with programmable logic and ASIC technologies Essential principles of Boolean algebra and combinational logic design with discussions of timing and hazards Core modeling techniques combinational building blocks buffers decoders encoders multiplexers adders and parity checkers Sequential building blocks latches flip flops registers counters memory and sequential multipliers Designing finite state machines from ASM chart to D flip flops next state and output logic Modeling interfaces and packages with SystemVerilog Designing testbenches architecture constrained random test generation and assertion based verification Describing RTL and FPGA synthesis models Understanding and implementing Design for Test Exploring anomalous behavior in asynchronous sequential circuits Performing Verilog AMS and mixed signal modeling Whatever your experience with digital design older versions of Verilog or VHDL this book will help you discover SystemVerilog's full power and use it to the fullest **Digital Design** William James Dally, R. Curtis Harting, 2012-09-17 This book provides students with a system level perspective and the tools they need to understand analyze and design complete digital systems using Verilog It goes beyond the design of simple combinational and sequential modules to show how such modules are used to build complete systems reflecting digital design in the real world

Computer Hardware Description Languages and Their Applications David Agnew, Luc J. M. Claesen, Raul Camposano, 1993 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by the increasing complexity of systems the growth of HDL driven synthesis the research on formal design methods and many other related advances This research oriented publication aims to make a strong contribution to further developments in the field The following topics are explored in depth BDD based system design and analysis system level formal verification formal reasoning on hardware languages for protocol specification VHDL HDL based design methods high level synthesis and text graphical HDLs There are short papers covering advanced design capture and recent work in high level synthesis and formal verification In addition several invited presentations on key issues discuss and summarize recent advances in real time system design automatic verification of sequential circuits and languages for protocol specification **Reuse Techniques for VLSI Design** Ralf Seepold, Arno Kunzmann, 2012-12-06 Reuse Techniques for VLSI Design is a reflection on the current state of the art in design reuse for microelectronic systems To that end it is the first book to garner the input of leading experts from both research and application areas These experts document herein not only their more mature approaches but also their latest research results Firstly it sets out the background and support from international organisations that enforce System on a Chip SoC design by reuse oriented methodologies This overview is followed by a number of technical presentations covering different requirements of the reuse domain These are presented from different points of view i e IP provider IP user designer isolated reuse intra company or inter company reuse More general systems or case studies e g metrics are followed by comprehensive reuse systems e g reuse management systems partly including business models Since

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approached in an ad hoc fashion Visually inspecting simulation results is no longer feasible and the directed test case methodology is reaching its limit Moore's Law demands a productivity revolution in functional verification methodology Writing Testbenches Using SystemVerilog offers a clear blueprint of a verification process that aims for first time success using the SystemVerilog language From simulators to source management tools from specification to functional coverage from I s and O s to high level abstractions from interfaces to bus functional models from transactions to self checking testbenches from directed testcases to constrained random generators from behavioral models to regression suites this book covers it all Writing Testbenches Using SystemVerilog presents many of the functional verification features that were added to the Verilog language as part of SystemVerilog Interfaces virtual modports classes program blocks clocking blocks and others SystemVerilog features are introduced within a coherent verification methodology and usage model Writing Testbenches Using SystemVerilog introduces the reader to all elements of a modern scalable verification methodology It is an introduction and prelude to the verification methodology detailed in the Verification Methodology Manual for SystemVerilog It is a SystemVerilog version of the author's bestselling book Writing Testbenches Functional Verification of HDL Models

Using PSL/Sugar for Formal and Dynamic Verification Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari, 2004

SystemVerilog Assertions Handbook Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari, 2005 **A Practical**

Approach to VLSI System on Chip (SoC) Design Veena S. Chakravarthi, 2022-12-13 Now in a thoroughly revised second edition this practical practitioner guide provides a comprehensive overview of the SoC design process It explains end to end system on chip SoC design processes and includes updated coverage of design methodology the design environment EDA tool flow design decisions choice of design intellectual property IP cores sign off procedures and design infrastructure requirements The second edition provides new information on SOC trends and updated design cases Coverage also includes critical advanced guidance on the latest UPF based low power design flow challenges of deep submicron technologies and 3D design fundamentals which will prepare the readers for the challenges of working at the nanotechnology scale A Practical Approach to VLSI System on Chip SoC Design A Comprehensive Guide Second Edition provides engineers who aspire to become VLSI designers with all the necessary information and details of EDA tools It will be a valuable professional reference for those working on VLSI design and verification portfolios in complex SoC designs **Modeling, Synthesis,**

and Rapid Prototyping with the Verilog HDL Michael D. Ciletti, 1999 Verilog aims to introduce new users to the language of Verilog with instruction on how to write hardware descriptions in Verilog in a style that can be synthesized by readily available synthesis tools Offers clear exposition of the Verilog hardware description language This book is written in a style that allows the user who has no previous background with hardware description languages HDLs to become skillful with the language Features treatment of synthesis friendly descriptive styles An excellent book for self study reference seminars and workshops on the subject FPGA/CPLD □□□□□□□□ □□, 2005 Xilinx Altera FPGA CPLD FPGA CPLD MAX plus II Quartus ISE

Verilog VHDL LED LCD ISA PCI FPGA CPLD Introduction to Microelectronics to Nanoelectronics Manoj Kumar Majumder, Vijay Rao Kumbhare, Aditya Japa, Brajesh Kumar Kaushik, 2020-11-24 Focussing on micro and nanoelectronics design and technology this book provides thorough analysis and demonstration starting from semiconductor devices to VLSI fabrication designing analog and digital on chip interconnect modeling culminating with emerging non silicon nano devices It gives detailed description of both theoretical as well as industry standard HSPICE Verilog Cadence simulation based real time modeling approach with focus on fabrication of bulk and nano devices Each chapter of this proposed title starts with a brief introduction of the presented topic and ends with a summary indicating the futuristic aspect including practice questions Aimed at researchers and senior undergraduate graduate students in electrical and electronics engineering microelectronics nanoelectronics and nanotechnology this book Provides broad and comprehensive coverage from Microelectronics to Nanoelectronics including design in analog and digital electronics Includes HDL and VLSI design going into the nanoelectronics arena Discusses devices circuit analysis design methodology and real time simulation based on industry standard HSPICE tool Explores emerging devices such as FinFETs Tunnel FETs TFETs and CNTFETs including their circuit co designing Covers real time illustration using industry standard Verilog Cadence and Synopsys simulations

Hardware Verification with System Verilog Mike Mintz, Robert Ekendahl, 2007-05-03 This is the second of our books designed to help the professional verifier manage complexity This time we have responded to a growing interest not only in object oriented programming but also in SystemVerilog The writing of this second handbook has been just another step in an ongoing masochistic endeavor to make your professional lives as painfree as possible The authors are not special people We have worked in several companies large and small made mistakes and generally muddled through our work There are many people in the industry who are smarter than we are and many coworkers who are more experienced However we have a strong desire to help We have been in the lab when we bring up the chips fresh from the fab with customers and sales breathing down our necks We ve been through software 1 bring up and worked on drivers that had to work around bugs in production chips What we feel makes us unique is our combined broad experience from both the software and hardware worlds Mike has over 20 years of experience from the software world that he applies in this book to hardware verification Robert has over 12 years of experience with hardware verification with a focus on environments and methodology

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