8-6 HDL Representation of the Binary Multiplier-Verilog

```
begin
  if (LOADB == 1)
     B <= MULT_IN;
  if (LOADO == 1)
     O <= MULT_IN;
  case (state)
     IDLE:
        if (G == 1)
          begin
             C <= 0;
             A <= 4'b0000;
             P <= 2'bl1;
           and
     MULLO:
        if (0[0] == 1)
           \{C, A\} = A + B;
     MILL 1:
        begin
           C <= 1'b0;
           A <= (C, A[3:1]);
           Q \leftarrow \{A[0], Q[3:1]\}:
           P <= P - 2'b01;
   endcase
end
endmodule
```

Figure 8-16 Verilog Description of a Binary Multiplier(Continued)

Verilog Code For Binary Multiplier

Joseph Cavanagh



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