



Fig. 8.31 Snapper. Icons (a) and circuit (b).

As it is impossible to indicate any dependency between an input and an output, no truth table can be given. A snapper is not a logic gate but the simplest form of an unlocked bistable. Snappers are also known as bus holders, holding amplifiers, and level retention devices.

Observation 8.8. *Its bistable nature notwithstanding, a snapper is not intended for data storage. Spurious signals such as glitches may cause a snapper to toggle at any time. Once driving of its terminal node has ceased, any state previously assumed must be regarded as corrupted.*

Much like any other bistable subcircuit, a snapper exhibits metastability when subjected to marginal triggering. For the memory loop to reliably snap into a new state, any data transition must reach a valid logic state and rest there for some minimum time. Timing conditions are, therefore, expressed in terms of minimum low and high times for the snapper's terminal.

8.4.2 Schmitt trigger

What sets Schmitt triggers apart from buffers and inverters is their hysteresis, see fig.8.32. As opposed to ordinary gates, the output is logically defined for any input voltage with no indeterminate or forbidden interval. Instead, distinct thresholds apply to rising and to falling input voltages, which means that a Schmitt trigger's output partly depends on past input.³²

$$U_{hF} = U_{ih} - U_{il} > 0 \quad (8.46)$$

Hysteresis is desirable in certain situations to obtain ample noise margins and/or better level restoration than ordinary buffers or inverters would provide. External inputs, for instance, are often passed through Schmitt triggers to filter out noise and to reshape waveforms. Three alternative circuit diagrams are shown in fig.8.33. Observe that positive feedback is essential in obtaining hysteresis and that its exact amount U_{hF} is a function of the transistor sizes involved. Figure 8.33b makes use of weaker-than-normal MOSFETs to obtain a limited degree of feedback whereas c and d can be designed to make do with minimum-length transistors.

³² The assignment of the mathematical symbols U_{ih} and U_{il} to a Schmitt trigger's pair of threshold voltages is debatable. Some sources of information assign them the other way round so that $U_{ih} < U_{il}$. With the definition $U_{hF} = U_{il} - U_{ih}$, a hysteresis of $U_{hF} < 0$ naturally follows for all regular gates and $U_{hF} > 0$ for Schmitt triggers. While this is meaningful, we prefer the assignment of fig.8.32 because U_{il} thus consistently defines the upper bound below which all input voltages get interpreted as logic 0, and vice versa for U_{ih} .

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Table of Contents Solution Manual Digital Integrated Circuit Hodges

1. Understanding the eBook Solution Manual Digital Integrated Circuit Hodges
 - The Rise of Digital Reading Solution Manual Digital Integrated Circuit Hodges
 - Advantages of eBooks Over Traditional Books
2. Identifying Solution Manual Digital Integrated Circuit Hodges
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Solution Manual Digital Integrated Circuit Hodges
 - User-Friendly Interface
4. Exploring eBook Recommendations from Solution Manual Digital Integrated Circuit Hodges
 - Personalized Recommendations
 - Solution Manual Digital Integrated Circuit Hodges User Reviews and Ratings
 - Solution Manual Digital Integrated Circuit Hodges and Bestseller Lists
5. Accessing Solution Manual Digital Integrated Circuit Hodges Free and Paid eBooks
 - Solution Manual Digital Integrated Circuit Hodges Public Domain eBooks
 - Solution Manual Digital Integrated Circuit Hodges eBook Subscription Services
 - Solution Manual Digital Integrated Circuit Hodges Budget-Friendly Options

6. Navigating Solution Manual Digital Integrated Circuit Hodges eBook Formats
 - ePub, PDF, MOBI, and More
 - Solution Manual Digital Integrated Circuit Hodges Compatibility with Devices
 - Solution Manual Digital Integrated Circuit Hodges Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Solution Manual Digital Integrated Circuit Hodges
 - Highlighting and Note-Taking Solution Manual Digital Integrated Circuit Hodges
 - Interactive Elements Solution Manual Digital Integrated Circuit Hodges
8. Staying Engaged with Solution Manual Digital Integrated Circuit Hodges
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Solution Manual Digital Integrated Circuit Hodges
9. Balancing eBooks and Physical Books Solution Manual Digital Integrated Circuit Hodges
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Solution Manual Digital Integrated Circuit Hodges
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Solution Manual Digital Integrated Circuit Hodges
 - Setting Reading Goals Solution Manual Digital Integrated Circuit Hodges
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Solution Manual Digital Integrated Circuit Hodges
 - Fact-Checking eBook Content of Solution Manual Digital Integrated Circuit Hodges
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements

- Interactive and Gamified eBooks

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